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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JUAN I. MARTINEZ, SCOTTY MARK WIGINTON,
and WILLIAM PAUL SWANEY

Appeal 2009-002619
Application 10/781,477
Technology Center 2100

Decided: February 22, 2010

Before JOSEPH L. DIXON, LANCE LEONARD BARRY, and THU A. DANG, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

The Patent Examiner rejected claims 1-30. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

INVENTION

Computer systems are prone to fault conditions that cause them to reboot. (¶ Par., [0001].) The Appellants' invention reports such reboots. (¶ Para., [0003].)

ILLUSTRATIVE CLAIM

1. A method of reboot reporting comprising:

reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors;

generating at least one non-maskable interrupt signal;

outputting the non-maskable interrupt signal to a processor of the plurality of computer systems;

outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems; and

generating an indication that at least one computer system has a fault condition.

PRIOR ART

Murthy	US 6,732,298 B1	May 4, 2004

REJECTION

Claims 1-30 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Murthy.

CLAIM GROUPING

In their Appeal Brief (p. 4), the Appellants stipulate that "[c]laims 2-4, 6-18, and 20-30 stand or fall with independent claim 1 . . . ." The

Appellants' Reply Brief, however, introduces new arguments about claim 1 not argued in their Appeal Brief and new arguments about claims 2-4 and 6-12.

ISSUE

Therefore, the issue is whether the Appellants have shown that we should consider their new arguments.

LAW

"[I]t is inappropriate for appellants to discuss in their reply brief matters not raised in . . . the principal brief[ ]. Reply briefs are to be used to reply to matter[s] raised in the brief of the appellee." *Kaufman Co. v. Lantech, Inc.*, 807 F.2d 970, 973 n* (Fed. Cir. 1986). "Considering an argument advanced for the first time in a reply brief . . . is not only unfair to an appellee but also entails the risk of an improvident or ill-advised opinion on the legal issues tendered." *McBride v. Merrell Dow & Pharms., Inc.*, 800 F.2d 1208, 1211 (D.C. Cir. 1986) (internal citations omitted).

> There are cogent reasons for not permitting an appellant to raise issues or arguments in a reply brief. Among them are the unfairness to the appellee who does not have an opportunity to respond and the added burden on the court that a contrary practice would entail. As the Tenth Circuit put it, permitting an appellant to raise new arguments in a reply brief "would be unfair to the court itself, which without the benefit of a response from appellee to an appellant's late-blooming argument, would run the risk 'of an improvident or ill-advised opinion, given [the court's] dependence . . . on the adversarial process for sharpening the issues for decision.'" *Headrick* [*v. Rockwell Int'l Corp.*], 24 F.3d [1272,] 1278 [(10th Cir. 1994)],

(quoting *Herbert v. Nat'l Acad. of Scis.*, 974 F.2d 192, 196 (D.C. Cir. 1992)).

Carbino v. West, 168 F.3d 32, 34-35 (Fed. Cir. 1999).

FINDINGS OF FACT ("FFS")

1. The explanation of the rejection of claims 1-4 and 6-12 in the Examiner's Answer (pp. 4-8) is identical to that in the Final Rejection (pp. 3-7).

ANALYSIS

Because the rejection that the Examiner makes in his Answer is identical to that in the Final Rejection (FF 1), from which the instant appeal was taken, we find nothing that would have prompted the new argument in the Reply Brief. The Appellants could have made the argument in their Appeal Brief. The term "reply brief" is exactly that, a brief in reply to new rejections or new arguments set forth in an Examiner's Answer. The Appellants may not present arguments in a piecemeal fashion, holding back arguments until an examiner answers the original brief. Of course, the Appellants may present new arguments directly to the Examiner for consideration as part of a continuing application.

CONCLUSION

Based on the finding of fact and analysis above, we conclude that the Appellants have not shown that we should consider the new arguments. Therefore, we will decide the appeal of claims 1-4, 6-18, and 20-30 based on claim 1 alone. *See* 37 C.F.R. § 41.37(c)(1)(vii).

CLAIMS 1-4, 6-18, AND 20-30

The Examiner finds that "Murthy discloses a method of reboot reporting comprising . . . [g]enerating at least one non-maskable interrupt signal; (Column 2; lines 61-62) . . . ." (Ans. 4.) The Appellants argue that "Murthy expressly discloses that its processor does not implement nonmaskable interrupts." (App. Br. 6.)

ISSUE

Therefore, the issue before us is whether the Appellants have shown error in the Examiner's finding that Murthy generat[es] at least one non-maskable interrupt ("NMI").

LAW

"It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim, and that anticipation is a fact question . . . ." *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.*, 730 F.2d 1452, 1457 (Fed. Cir. 1984)). Of course, anticipation "is not an 'ipsissimis verbis' test." *In re Bond*, 910 F.2d 831, 832-33 (Fed. Cir. 1990) (citing *Akzo N.V. v. United States Int'l Trade Comm'n*, 808 F.2d 1471, 1479 n.11 (Fed. Cir. 1986)). "An anticipatory reference . . . need not duplicate word for word what is in the claims." *Standard Havens Prods. v. Gencor Indus.*, 953 F.2d 1360, 1369 (Fed. Cir. 1991).

FINDINGS OF FACT

2. Figure 2 of Murthy follows.

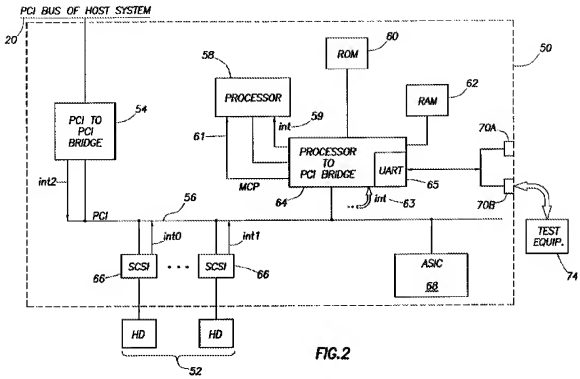

FIG.2

The reference explains that "FIG. 2 shows the preferred structure of a disk array controller 50 . . . . As shown, the disk array controller 50 preferably includes . . . a disk array processor 58 . . . [and] a processor-to-PCI bridge 64 . . . ." (Col. 5, ll. 19-24.)

3. "In addition to or instead of using MCP [i.e., machine check exception] line 61 in accordance with its intended use (i.e. to notify processor 58 of a catastrophic failure on the hardware board), the processor-to-PCI bridge 64 uses the MCP line 61 as a nonmaskable, pseudo-interrupt." (Col. 6, ll. 32-36.)

4. The reference includes the following explanation about the operation of the nonmaskable, pseudo-interrupt.

> A pseudo-interrupt asserted on MCP line 61 to processor 58 at any time by test equipment 74 informs the processor of a critical failure requiring service independent of various device interrupts. After the MCP line is asserted, the processor calls an interrupt handler that executes software to service the machine check exception. Even if all device interrupts in the processor 58 are disabled, a pseudo-interrupt may be generated by asserting the MCP line using the communication software in the laptop connected through connectors 70A or 70B to the processor-to-PCI bridge 64. This nonmaskable pseudo-interrupt workaround permits debugging even if all interrupts in processor 58 have been disabled and a hardware failure has occurred on the array controller board 50 which has completely "hung" the system . . . .

(*Id.* at ll. 36-50.)

5. "The result is that a processor 58 that has no equivalent to a nonmaskable interrupt (NMI) (a NMI is an interrupt which cannot be disabled) capability is effectively given such a capability." (*Id.* at ll. 17-20.)

ANALYSIS

Murthy discloses a disk array controller 50 that includes a disk array processor 58 and a processor-to-PCI bridge 64. (FF 2.) Figure 2 of the reference shows an MCP line 61 connecting the processor and bridge. (*Id.*) In addition to or instead of using the MCP line to notify the processor of a catastrophic failure on the hardware board, the bridge 64 uses the line as a nonmaskable, pseudo-interrupt. (FF 3.)

A pseudo-interrupt asserted on the MCP line to the processor by test equipment 74 informs the processor of a critical failure requiring service independent of various device interrupts. After the MCP line is asserted, the processor calls an interrupt handler that executes software to service the machine check exception. (FF 4.) This nonmaskable pseudo-interrupt workaround permits debugging even if all interrupts in the processor have been disabled. (*Id.*) The result is that the processor, which originally had no equivalent to a NMI capability is effectively given such a capability. (FF 5.)

We agree with the Examiner that "[t]he fact that Murthy called these non-maskable interrupts non maskable pseudo interrupt[s] is irrelevant . . . because an interrupt when implemented is an interrupt whether it is called pseudo or something else." (Answer 16.) "In other words, a result of implementing interrupts or pseudo interrupts within a processor is the same. The result is to call an exception, and execute an exception routine . . . ." (*Id.*)

CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Appellants have shown no error in the Examiner's finding that Murthy generates at least one NMI.

CLAIMS 5 AND 19

The Examiner finds that "[i]t is evident that while Murthy labels the generated interrupts as int0, intl, int2, Murthy also counts the interrupts by counting the label 0,1,2." (Ans. 17.) The Appellants argue that "it is

respectfully submitted that the relied upon disclosure does not teach or suggest the 'counting . . .' limitation . . . . " (App. Br. 7.)

ISSUE

Therefore, the issue before us is whether the Appellants have shown error in the Examiner's finding that Murthy counts the number of times the NMI is generated.

LAW

"The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not . . . resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis." *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967).

FINDING OF FACT

6. Murthy includes the following disclosure.

> As shown in FIG. 2, various interrupts (int 0, int 1, int 2 . . .) are generated by the devices given in FIG. 1 and FIG. 2 and are handled by processor 58. The interrupts are used by various devices on the array controller 50 to request service from processor 58.

(Col. 6, ll. 21-25.)

ANALYSIS

Figure 2 of Murthy shows various interrupts that are generated by the devices handled by the processor 58. The interrupts are used by the various devices on the array controller 50 to request service from the processor. (FF 6.) Speculations or assumptions would be required, however, to find that

Murthy counts the interrupts by counting the label 0, 1, 2. Instead, we agree with the Appellants that "the listing of 'int0,' 'intl,' and 'int2' are reference labels to separate system components shown in Fig. 2 of Murthy, not to a process step counting the number of times a non-maskable interrupt signal is generated . . . . " (App. Br. 7.)

CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Appellants have shown error in the Examiner's finding that Murthy counts the number of times the NMI is generated.

DECISION

We affirm the rejection of claims 1-4, 6-18, and 20-30. In contrast, we reverse the rejection of claims 5 and 19.

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

rwk

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